REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1 and 3-29 are now in the application. Claims 1, 3-12 and 29 are subject to examination and claims 13-28 have been withdrawn from examination. Claims 1, 3 and 9 have been amended. Claim 29 has been added. Claim 2 has been canceled. It is noted that item 4 of the Office Action Summary is incorrect in that it lists only claims 1-12 as pending.

In "Claim Rejections - 35 USC § 102", item 3 on pages 2-3 of the above-identified Office Action, claims 1, 5 and 8 have been rejected as being fully anticipated by U.S. Patent No. 4,106,049 to Shinozaki et al. (hereinafter Shinozaki) under 35 U.S.C. § 102(b).

In "Claim Rejections - 35 USC § 103", item 5 on pages 3-4 of the Office Action, claims 2-4 and 6 have been rejected as being obvious over Shinozaki under 35 U.S.C. § 103(a).

In "Claim Rejections - 35 USC § 103", item 6 on pages 4-5 of the Office Action, claims 7 and 9-12 have been rejected as being obvious over Shinozaki in view of U.S. Patent No. 5,866,943 to Mertol under 35 U.S.C. § 103(a).

As will be explained below, it is believed that the claims were patentable over the cited art in their original form. Nevertheless, claims 1 and 9 have been amended and claim 29 has been added to make this even clearer. Support for the changes to the claims is found in original claims 2, 18 and 26 and on pages 25 and 26 of the specification, of the instant application.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*, an electronic component with shielding against stray electromagnetic fields, the electronic component comprising:

> a ground potential terminal for receiving an external ground potential;
>
> a semiconductor chip having a semiconductor substrate with an active upper side and a passive rear side having a surface area;
>
> at least one ground lead disposed within said semiconductor substrate and having at least one contact area contacting said upper side of said semiconductor substrate for connecting to said ground potential terminal; and
>
> a continuous electrically conductive buried layer having a surface area corresponding in size to said surface area of said passive rear side and entirely extending over said surface area, said buried layer disposed within said semiconductor substrate adjacent said passive rear side and connected to said ground potential terminal through said ground lead for <u>providing a rear</u>

side shielding with said buried layer, and said buried layer being formed of a semiconductor material doped with an impurity concentration of over 1×10^{20} cm^{-3}.

The Shinozaki reference discloses a semiconductor device having a p+ silicon substrate 11, a p- layer 12 on the substrate and an n+ buried layer 13 in the layer 12, as is seen in Fig. 1 and described in column 3, lines 1-52 of the reference. In particular, column 3, lines 48-49 state that the buried layer 13 is of the n+ type. A similar structure is shown in Fig. 5 of Shinozaki. Fig. 2 illustrates a pnp transistor Q2 and an npn transistor Q1.

It is important to note that the buried layer 13 of Shinozaki is not a shield. The layer 13 in Shinozaki is an electrode and at the same time a base of the transistor Q2 and an emitter of the transistor Q1, as is disclosed in column 3, line 46 et seq. of Shinozaki. In fact, the layer 13 is positively doped, like layer 11. This function also applies to Fig. 5 which has been expressly mentioned in the Office action.

In the semiconductor device of the invention of the instant application, the buried layer acts as a shield, meaning that its conductivity should be very high, near that of metal. Claim 1, even in its previous form, called for "providing a

rear side shielding with said buried layer."

In order to make the differences between Shinozaki and claim 1 of the instant application even clearer, the subject matter of claim 2 has been added to claim 1. Therefore, claim 1 now contains a lower limit of over 1×10^{20} cm^{-3} for the impurity concentration.

This even further clarifies the difference between the subject matter of the invention and the state of the art. According to claim 1 of Shinozaki, the "second" (buried) layer has an impurity concentration intermediate that of the substrate (see claim 6 of Shinozaki) and the first layer (see claim 7 of Shinozaki) and therefore is orders of magnitude lower than in the invention of the instant application as claimed.

Applicants cannot follow the argumentation of the Examiner with regard to the feature previously recited in claim 2 and now in claim 1. Nothing in Shinozaki contains any suggestion to further increase the impurity concentration since the concentration claimed in Shinozaki is appropriate for the purpose underlying the buried layer used therein.

However, the invention of the instant application has a different object, and it has been found by the inventors of the instant application that for the best results the concentration should be very high. Again, it must be pointed out that the buried layer of the invention of the instant application does not serve any function of an electrode of a vertical transistor, but only serves to shield against stray fields.

Therefore, radio-frequency is a proper field of application for the invention of the instant application as recited in claim 8.

Regarding the rejection of claims 7 and 9-12 over a combination of Shinozaki and Mertol, it is noted that while flip-chip mounting is, of course, customary per se, without having to refer to Mertol, in ultra high frequency applications, devices as illustrated in Fig. 2 and particularly Fig. 3 of the instant application are well suited because there are only very short connections and the device is shielded not only from above by the buried layer but also from below by a shielding ground-carrying line (22) connected to the solder formations or contact area, as is now recited in amended claim 9 and new claim 29 of the instant application. As mentioned above, the shielding ground-

carrying line is found in original claims 18 and 26 and pages 25 and 26 of the instant application. Certainly, such a feature is not found in the prior art.

Clearly, Shinozaki and Mertol do not show providing a rear side shielding with a buried layer, and the buried layer being formed of a semiconductor material doped with an impurity concentration of over 1×10^{20} cm^{-3}, as recited in claim 1, nor a shielding ground-carrying line as recited in claims 9 and 29, of the instant application.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 1, 9 and 29. Claims 1, 9 and 29 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1.

In view of the foregoing, reconsideration and allowance of claims 1, 3-12 and 29 are solicited. Rejoinder of method claims 13-28 are also requested under MPEP 821.04.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a

telephone call so that, if possible, patentable language can be worked out.

If an extension of time is required, petition for extension is herewith made. Any extension fee associated therewith should be charged to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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